REMARKS

Claims 1, 3 and 4 have been amended. Support for the amendments can be found at FIG. 9 of the present application. Claims 1-4, 7 and 8 are pending and under consideration.

I. REJECTION OF CLAIMS 1-4 UNDER 35 U.S.C. § 103(a) AS BEING UNPATENTABLE OVER KAMETANI ET AL. (EP 400328A; HEREINAFTER "KAMETANI") IN VIEW OF LEWIS (US PATENT NO. 6,378,066):

For clarification purposes, claim 1 has been amended to recite "an information processing method for causing a computing device having a plurality of processors to carry out predetermined information processing, the information processing method comprising...comparing a first parallel block number of a parallel processing control information region corresponding to a parallel processing block executed by a foremost thread and a second parallel block number of a thread information region which corresponds to the respective thread assigned to the predetermined processor [and] determining whether a corresponding thread of the predetermined processor should execute said next parallel processing block based upon the comparison results, wherein when execution is required, determining said next parallel processing block to be executed by the predetermined processor with reference to said second parallel block number, and generating a parallel processing block control information region corresponding to said next parallel processing block, wherein a number of threads executed in said next parallel processing block are stored, and said corresponding thread of the predetermined processor executing said next parallel processing block..."

At page 3 of the Office Action, the Examiner admits that Kametani fails to disclose all of the features recited in claim 1. However, the Examiner asserts that Lewis makes up for the deficiencies of Kametani.

The Applicants respectfully submit the Lewis fails to disclose "comparing a first parallel block number of a parallel processing control information region corresponding to a parallel processing block executed by a foremost thread and a second parallel block number of a thread information region which corresponds to the respective thread assigned to the predetermined processor... [and] determining whether a corresponding thread of the predetermined processor should execute said next parallel processing block..." as recited in amended claim 1.

Instead, FIG. 9 of Lewis discloses a method and apparatus for designing a data flow

program for execution in a multiprocessor computer system. Specifically, threads are assigned to a plurality of processors and if a thread is available to process a block corresponding to a specified program code, the thread determines whether there are any blocks in a queue and if so, the available thread selects a block from queue for processing (see column 9, lines 67 – column 10, lines 44). Further, if the thread determines that a selected block is dependent upon the execution of program code with respect to other blocks that have not been executed, the thread skips the selected block. Otherwise, if the block dependencies have been satisfied, the thread uses an assigned processor to execute the program code associated with that block.

The teaching of Lewis is fundamentally different from that of the claimed invention. The present invention relates to a thread being able to proceed to a next block without having to wait for the remaining threads to execute a block already executed by the thread. However, Lewis discloses a thread being able to skip a block if the block is dependent upon other blocks (see FIG. 9).

Therefore, the combination of Kametani and Lewis fails to establish a prima facie case of obviousness over the claimed invention.

Although the above comments are specifically directed to claim 1, it is respectfully submitted that the comments would be helpful in understanding differences of various other rejected claims over the cited reference.

Accordingly, claims 1-4 patentably distinguish over Kametani in view of Lewis. Therefore, it is respectfully submitted that the rejection is overcome.

II. REJECTION OF CLAIMS 7 AND 8 UNDER 35 U.S.C. § 102(e) AS BEING ANTICIPATED BY LEWIS:

The comments mentioned above, may also be incorporated here, where applicable, to address the rejection of claims 7 and 8.

Thus, claims 7 and 8 patentably distinguish over Lewis. Therefore, it is respectfully submitted that the rejection is overcome.

III. CONCLUSION:

In view of the foregoing amendments and remarks, it is respectfully submitted that each of the claims patentably distinguishes over the prior art, and therefore, defines allowable subject matter. A prompt and favorable reconsideration of the rejection along with an indication of

allowability of all pending claims are therefore respectfully requested.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

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By: _____
Deidre M. Davis
Registration No. 52,797

1201 New York Ave, N.W., Suite 700
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501